Design of Low Power Reversible Logic Gate based Adder / Subtractor

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Abstract:

Reversible logic has demonstrated potential in recent years as a method for optical computing, quantum computing, nanotechnology, and low-power VLSI design. The performance and dependability of digital systems that are now constructed with reversible logic gates can be improved. These gates speed up processing since they use less energy and have shorter quantum delays. In the present system, a low-power FinFet enabled complete adder and subtractor circuit is being developed. FinFets are created using a layout approach that maintains low power consumption by altering the bias voltage. The suggested system employs the reversible gate to construct a low-power reversible logic gate. The leakage voltage travelling across the crucial path is blocked by the reversible circuit. Afulladder/subtractor is implemented using a reversible logic gate based design.

Key words:

Reversible Logic Gates, Fin-Fet, CMOS, Adder , Subtractor

Introduction:

Landauer states that for each bit of information lost during irreversible computing, KTln2 Joules of heat energy are created, where K is the Boltzmann constant and T is the absolute temperature. The amount of heat dissipated at room temperature T is minimal (2.9X10-21 J), but not insignificant. This sum may appear insignificant at first, but it will become substantial in the future. Reversible computation would not result in this energy waste because doesn't have information loss.

Reversible logic gates are allow reversible circuits to maintain a onetoone mapped between inputs and outputs at all the times. In reversible circuits, there exist outputs that are used in subsequent computing stages but are not necessary for recovering any of the original inputs. These unnecessary outputs are waste outputs. Constant inputs (0 or 1) are used to hold interim values during processing in reversible quantum circuits. Reversible logic gates like Fredkin, Toffoli, Feynman, and Peres, among others, are used to create reversible circuits. Reversible

logic has a wide range of uses in emerging technologies such ultra-low power VLSI, optical computing, cellular automata, and quantum computers. Reversible logic gates are a crucial part of many computing systems, in general. The reversible logic gate accomplishes the goal of lower logic circuit power consumption by logically reusing logic information bits in comparison to conventional gates, reducing information bit use loss.

To remain reversible, a reversible logic gate must create a one to one mapped between its inputs and outputs. Stated simply, the inputs and outputs of a reversible gate are bijective. It aids in both recovering the inputs from the outputs in a unique method as well as extracting the outputs from the inputs. In this work, we suggested a reconfigurable signal generator application and a complete adder/subtractor based on Fredkin gates in a single circuit with mode selection.

Methodology

Reversible Logic Gates:

In the conventional method, every digital function is irreversible. Previous computations cannot be restored at any moment. Reversible operations could be used to carry out the computation's necessary tasks, generating no heat in the process. The input and output of any circuit must match for it to be reversible, which is one requirement. It is distinct from one another or mapped one to one. The second requirement is whether a gadget can when anything can physically run backwards, it is said to be reversible. Feynman Gate 2 is a basic reversible gate 3 x 3, Peres Gate 3 x 3, TSG gate 4 x, Fredkin Gate 3 x 3, Toffoli Gate 3 x 3, Double Feynman Gate 3 x 3. Other applications can potentially make use of the same gates.

The fundamental components of reversible circuits are reversible gates. Every input vector becomes a distinct output vector in a reversible circuit, and vice versa. Many fields find use for reversible circuits: digital signal processing, optical computation, DNA computing, bioinformatics, low power CMOS systems, nanotechnology-based systems, quantum computers, and communications. Equal numbers of inputs and outputs are necessary for reversible computation, as is the mapped of each input pattern to a unique output pattern and the availability of sufficient output values to retrieve the input values. Therefore, fan-out, feedback, and looping are forbidden. When designing a reversible circuit, the least amount of reversible gates, constant inputs, garbage outputs, and quantum costs should all be avoided. Among the fundamental parts of reversible computers are arithmetic logical units, multiplexers, and decoders.

Many computer units are built around a foundation of arithmetic adders and subtractors. Constructing adders and subtractors in a manner compatible with quantum computing and the anticipated paradigm shift logic is necessary. Other logical operations like division and multiplication can also be performed using them. In, a procedure for building a reversible complete adder with two RG gates is provided. To reduce the quantum cost, a reversible full adder with two Peres gates is implemented. Four Fredkin gates are the foundation of a powerful

full adder circuit that is introduced. An optical reversible full adder and subtractor made up of two NR gates is constructed using the NR gate, a novel type of reversible gate. It presents the MOG gate, a cutting-edge 4 by 4 reversible gate that functions as a complete adder and subtractor on its own. One Fredkin gate, one Peres gate, and two C gates make up the MOG gate. Two HNG gate-based designs and one Feynman gate-based design are presented.

Proposed Method

Implementation of Adder / Subtractor:

An adder/subtractor is a circuit that, by altering a control input, may execute either addition or subtraction. Combining adder and subtractor circuits into one circuit can save a large amount of space on the silicon area. Adder/subtractor circuits are part of the data processing system's arithmetic unit, or ALU. This circuit is used by the ALU to execute addition, addition with carry, increment, subtraction, decrement, and other operations. In several Digital Signal Processing applications, dedicated Adder/Subtractor circuits are required.

A comprehensive adder/subtractor is constructed in a current design utilising two Feynman and two Peres gates. When the control input is set to logic 0, addition is carried out, and when it is set to logic 1, subtraction is carried out. The quantum cost of the current design is 10. One steady input and three trash outputs are present. Ripple carry adder/ripple borrow subtractor circuits of different bit lengths can be constructed by cascading one-bit adder/subtractor circuits.

In this proposed architecture, a full adder/subtractor is built using two Feynman gates and one HNG gate. When the control input is set to logic 0, addition is permitted; when set to logic 1, subtraction is possible. The proposal has an 8 design quantum cost. One constant input and three garbage outputs are present. Different bit length ripple carry adder/ripple borrow subtractor circuits can be created by cascading one-bit adder/subtractor circuits.

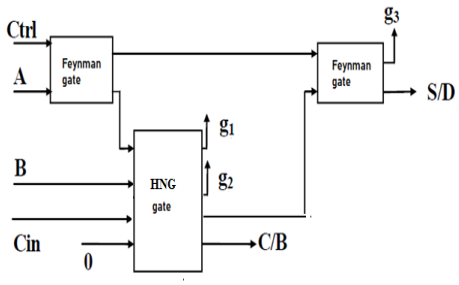

Figure 1: Proposed Adder/Subtracter circuit

Result and Discussion

A design of adder and subtractor using reversible logic gate isimplemented using the HNG and Feynman gate. Then the detailedanalysis of power , timing and device utilization summaries are discussed.

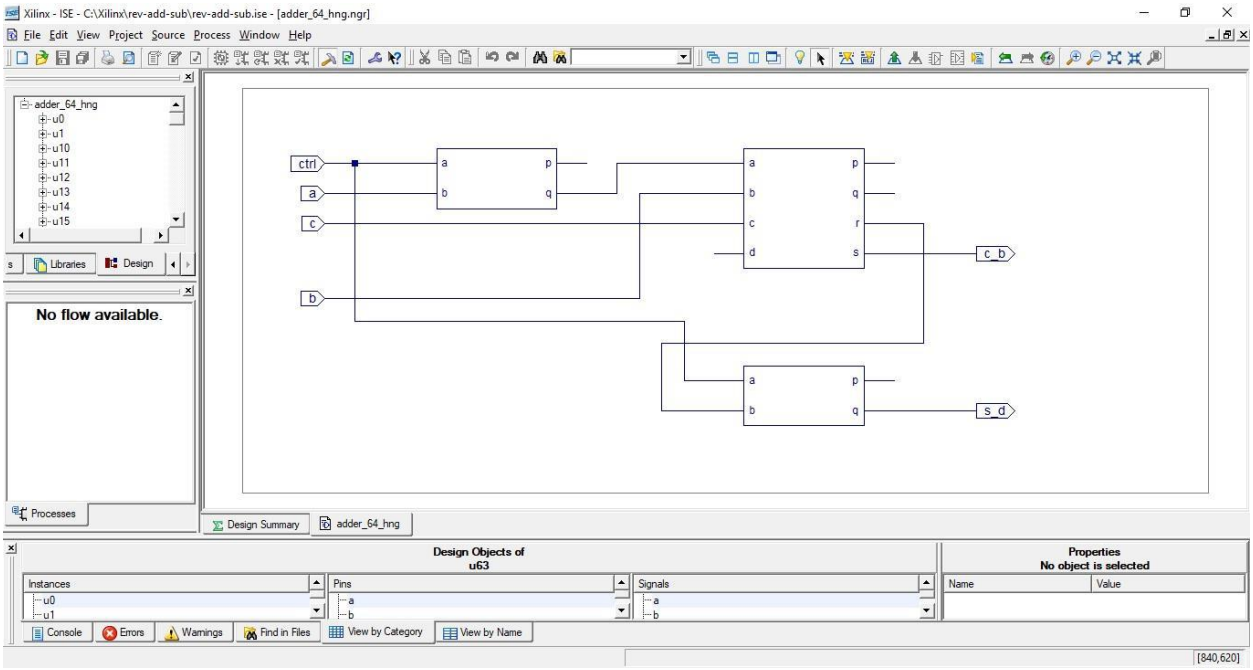

Figure 2: RTL Schematic Diagram

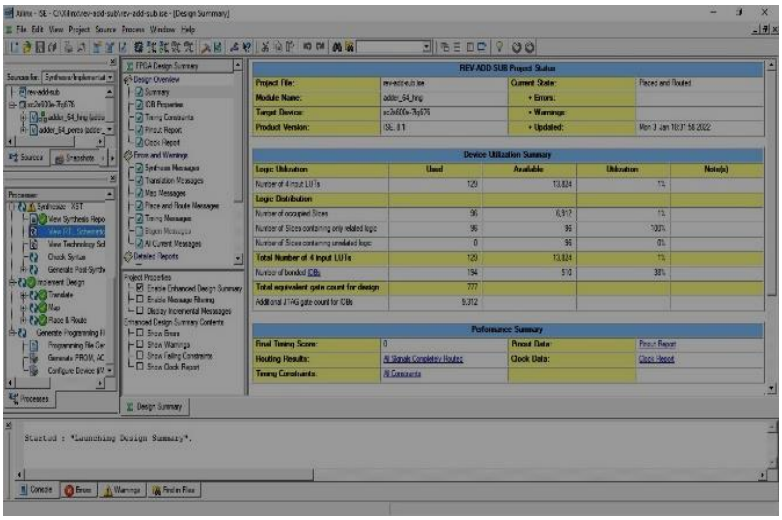

Figure 3: Device Utilization Summary of Proposed Method.

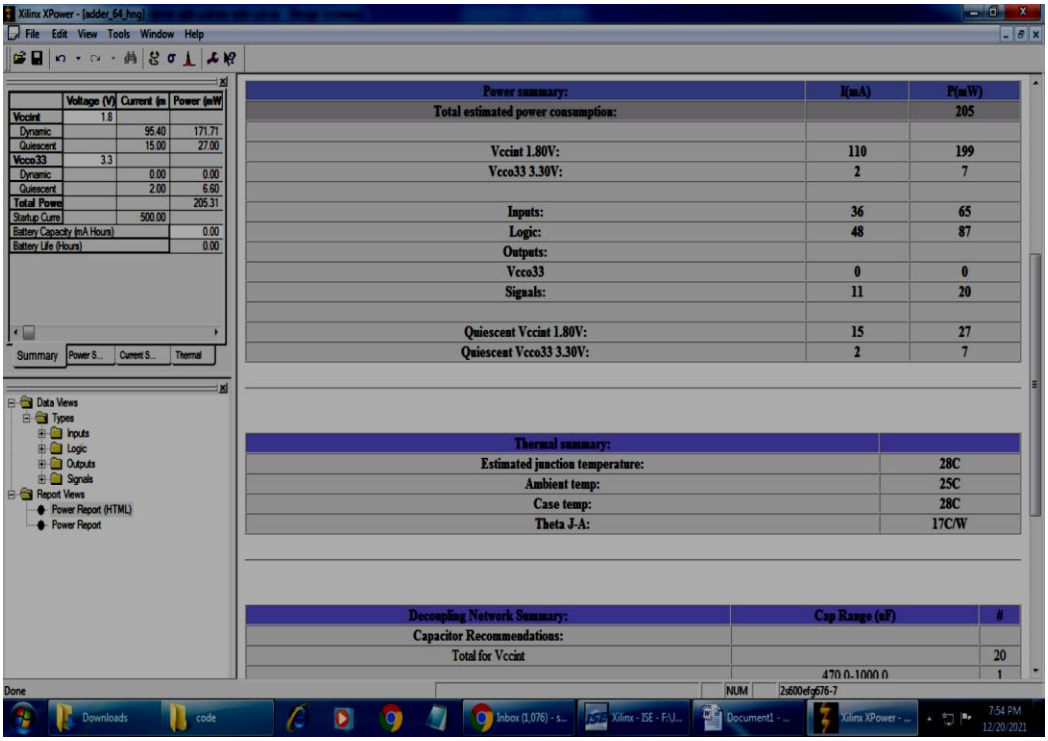

Figure 4: Power summary of proposed method

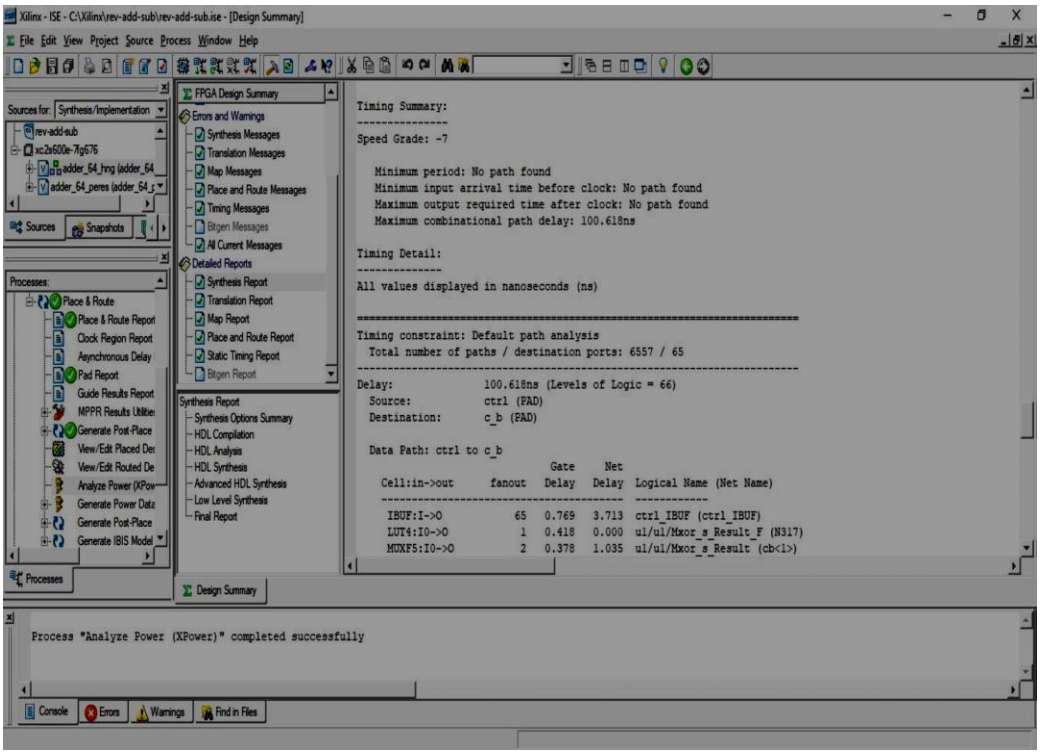

Figure 5:Time Summary of Proposed method

Table 1: Device Utilization Summary

Parameters	Existing	Proposed
Gate Count	256	192
Constant Input	64	64
Garbage Output	192	162
Quantum Cost	640	512
Power(mw)	224.44	205.31
Delay(ns)	110.126	100.618
LUTs	130	129

Conclusion

An adder/subtractor design has been published for this technique. By cascading n 1-bit circuits together, these designs can be utilised to construct n-bit adder/subtractor circuits. The Xilinx tool was used to simulate, analyse, and verify the designs. We study leaf cells, LUTs, quantum cost, trash output count, and nets. The simulation's findings show that the suggested architecture uses FPGA more efficiently than the systems that are currently in parameters, power consumption, and latency incurred. The recommended method makes it possible to swiftly construct an entire reversible computer architecture. In the near future, calculators, cell phones, and other low-power gadgets are anticipated to incorporate reversible adder/subtractor circuits. In addition, sequential reversible circuits, multipliers, ALUs, etc. can be built using the suggested adder/subtractor is implemented.

Abbreviations
Nil

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Author contribution

All Authors contributed entire manuscript in writing, reviewing, implementing and analysis.

Conflict of interest
The authors declare no conflict of interest.

Ethics approval
The research does not involve human participants.

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