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AN OPTIMIZED IMPLEMENTATION OF SYSTOLIC ARRAY BASED REVERSIBLE CIRCULAR CONVOLUTION ON FPGA

F.Mhaboobkhan, Assistant Professor
Department of ECE
P. A. College of Engineering and Technology
Pollachi, Coimbatore
khanmhaboob@gmail.com

M. Durga devi, U.G Scholar
Department of ECE
P. A. College of Engineering and Technology
Pollachi, Coimbatore
durgadevi982000@gmail.com

M. Kaaviyaa , U.G Scholar
Department of ECE
P. A. College of Engineering and Technology
Pollachi, Coimbatore
kaaviyaamylsamy@gmail.com

G.Keerthana, U.G Scholar
Department of ECE
P. A. College of Engineering and Technology
Pollachi, Coimbatore
Keerthanaganesan938@gmail.com

***Abstract*: Reversible logic is an emerging technology that does not have information loss and can be used where faster computations are necessary. Circular Convolution is a mathematical operation used in most of DSP and Image processing applications as an integral part, hence designing them effectively is mandatory. Systolic systems replace pipelined versions with an array of Processing components to perform recurring processes with a higher degree of regularity (PE).In this project a Reversible Circular Convolution (RCC) based on matrix method which makes use of Systolic array architecture has been proposed. The functionality of the convolution architecture that contains reversible carry save multiplier and reversible adder in RPE has been verified using Modelsim 5.7g. Gate counts, quantum cost, and garbage production have all been compared and tabulated as part of the parameter study and Hardware utilization were analyzed using Quartus-II 9.0 with respect to Cyclone-II device along with EP2C70F896C8 family.It was found that in proposed convolution architecture reversible gate count, quantum cost, and garbage outputs were improved by 58.89% , 62.09%, 69.37% respectively. Moreover, the logic utilization of Reversible Circular convolution Architecture (RCA) among 3*1, 4*1, 5*1 and 6*1 is 35.07%, 22.28%, 14.17%, and 16.40% respectively.**

Keywords: Carry save adder, Carry save multiplier, Parity preserving, Reversible logic, Ripple carry adder.

I. INTRODUCTION

Because of its capacity to lower power consumption, which is a major criterion in low-power VLSI design, reversible logic has attracted a lot of interest in recent years.Convolution is a technique for merging two signals into a single signal. When the impulse decomposition approach is utilised, systems are defined by a signal called the impulse response. Circular convolution is the convolution of two periodic functions with the same period. Processing Elements in a systolic design produce and pass data in a predictable order. It is designed to work as a co processor with a host computer, and its behaviour is modelled after blood flow through the heart, hence the name ,SYSTOLIC ARRAY. Every CPU sends and receives data on a regular basis, doing a small computation each time to keep the network running smoothly. On systolic networks with an array structure, many simple matrix calculations may be pipelined simply and effectively. Hexagonally connected computers, for example, could perform the maximum level of matrix multiplication possible.

REVERSIBLE LOGIC AND PARITY PRESERVING

Reversible logic can be utilized to avoid data loss during operations and is also employed in upcoming technologies such as Digital Signal Processing etc… The parity-preserving property is most commonly utilized in digital systems and allows a circuit to identify permanent and transient errors by comparing input and output parity. Parity-preserving gates with the input parity equal to the output parity can be used to create this fault tolerant/detection approach. The paper is structured as follows; Section II reviews a few reversible logic primitives including some performance measures. The reversible gates used in this proposed unit are described in Section III. In Section IV, the systolic array architecture and major reversible components are briefly addressed. . Section VI discusses the findings, and Section VII wraps up the research with a list of references.

II. REVERSIBLE LOGIC PRIMITIVES:

Irreversible logic gates are the most commonly utilised logic gates (AND, OR, NAND, NOR, XOR, and XNOR). Reversible gates were invented by Feynman, Toffoli, Peres,

Fredkin, HNG, and TSG, among others. The number of inputs and outputs determines the type of gate.

A.Quantum cost:

The quantum cost of a reversible gate is determined by the number of 1x1 to 2x2 reversible gates or quantum gates employed in the design. The quantum cost of all reversible 1x1 and 2x2 gates is considered to be the same [1].

B.Garbage outputs:

Garbage outputs are unused reversible circuit outputs[1].

C.Constant input:

When a logical 0 or 1 is used as the input to a reversible circuit, it is referred to as constant input. The reversible circuit's gates control the garbage outputs and constant inputs [1].

III.REVERSIBLE GATES

The reversible gates used in this paper are

1. P2RG
2. Fredkin

P2RG:

The P2RG, a 55-parity-preserving reversible gate, is depicted in Fig 1. Because one of its inputs is also an output, this gate is also known as a one through. When the input B and D are given as constant 1 and 0, the gate performs NOR operation. The NOR gate can be used to verify any Boolean function because it is a universal gate. The Quantum cost of a P2RG gate is 10.[4]

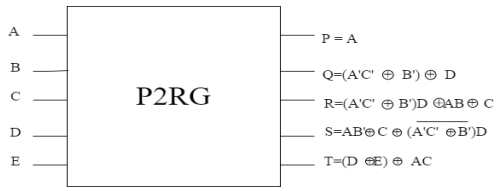

Fig. 1 P2RG Gate

Fredkin:

Fig 2 shows a reversible 3x3 Fredkin gate.

Fig 2 shows a reversible 3x3 Fredkin gate. The output of the first bit is directly provided. The last two bits are switched when the first bit is 1.

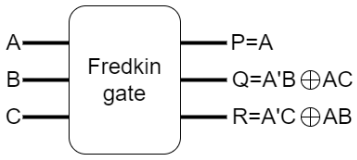

Fig. 2 Fredkin Gate

It's a universal gate that can do operations like AND, NOT, and OR. The output is defined by P=A, Q=((~A).B)+(A.C) ; and R=(A.B)+((~A).C) . Quantum cost of a Fredkin gate is 5 [4]

Parity preserving Full Adder

One P2RG gate and one Fredkin gate are used to create the parity-preserving Full Adder/Subtractor depicted in Fig.3.A, B and Cin are the three inputs. A control line directs the operation to be performed. The addition is performed when the control line is logical 0.When the control line is logical 1, subtraction is conducted.

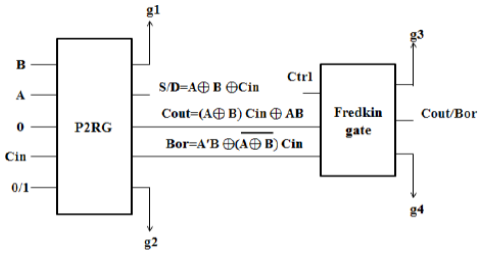

Fig. 3 Full adder/Subtractor

.

The whole adder's Boolean equations are illustrated below, with three constant inputs and four trash outputs.

Sum=A⊕B⊕C
Carry= ((A⊕B) Cin) ⊕AB
Borrow= ((A)'B) ⊕ (((A⊕B)') Cin))

IV.CONVOLUTION

convolution is crucial in signals and systems because it connects the input signal with the system's impulse response to produce the output signal.

TYPES OF CONVOLUTION:

a. Linear convolution
b. Circular convolution

METHODS OF CIRCULAR CONVOLUTION :

In general, there are two approaches for performing circular convolution:

1. Concentric circle method,
2. Matrix multiplication method

In this paper, matrix multiplication approach to build a reversible circular convolution has been implemented.

I. The matrix approach depicts the two provided sequences as a matrix.

II. One of the given sequences is repeated, one sample at a time, to create a N X N matrix.

III. The other sequence is represented as column matrix.

IV. Circular convolution is accomplished by multiplying two matrices.

In comparison to linear convolution, circular convolution benefits from discrete and finite signals. Therefore linear convolution isn't feasible.

V.SYSTOLIC ARRAY ARCHITECTURE

A two dimensional square array is shown in Fig.4. Systolic systems are made up of an array of RPE (Reversible Processing Elements) processors, known as cells. In a mesh-like structure, each cell is connected to a limited number of surrounding cells.

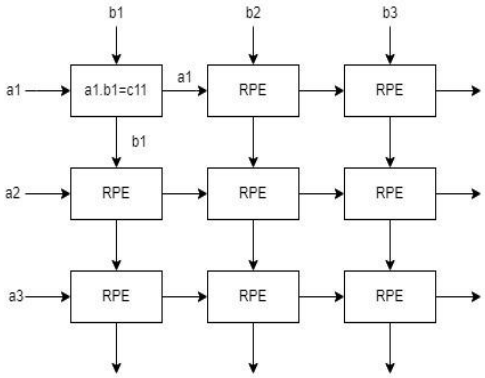

Fig.4 Two-dimensional square array

In a systolic array, a large number of identical simple processors (RPE) are put in a well-organized structure such as a linear or two-dimensional array. Each RPE is connected to the others and has a limited amount of private storage.
Each cell Cij of the matrix multiplier receives its ai and bi operands from the left and top, respectively. In addition to computing z, Cij propogates its ai and bi input operands rightward and downward, respectively. The systolic matrix multiplier is constructed from n(2n-1) copies of Cij, which are connected in the two dimension mesh configuration . As in a one-dimensional pipeline, the end operands constituting the ith row of ai flow horizontally from left to right via the ith row of cells.

INTERNAL ARCHITECTURE OF RPE

A Reversible Carry Save Multiplier and Reversible Carry Save Adder make up RPE's internal design.

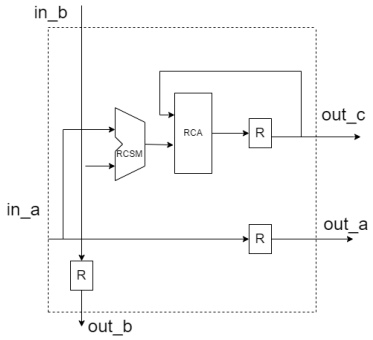

Fig .5 Internal architecture of RPE

Fig.5 depicts RPE's internal architecture. In Reversible processing element block initially two inputs namely in_a , in_b is fed to carry save multiplier, it multiplies both of the inputs and its output act as an one of the input to the carry save adder another output of the adder block is fed back from its output and both of values get added and finally result get stored in out_c. out_a and out_b is given as an input for next RPE block, through row wise and column wise respectively.

A.REVERSIBLE CARRY SAVE MULTIPLIER

As seen in Fig.6, this unit employs a reversible carry save multiplier. Using an array of Carry Save Adders, the Carry Save Multiplier accumulates partial product. It's also one of the high-speed multipliers with two input AND gates and a reversible complete adder in each block , as shown in Fig 7.

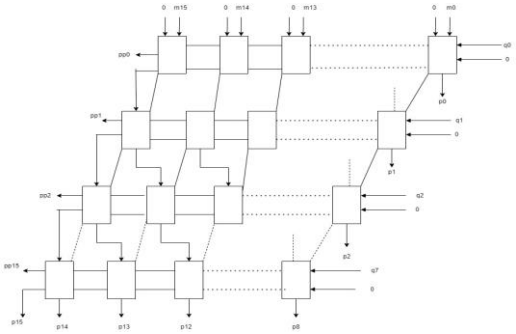

Fig. 6 Carry save multiplier

INTERNAL ARCHITECTURE OF CSM

Fig.7 depicts the internal architecture of CSM.

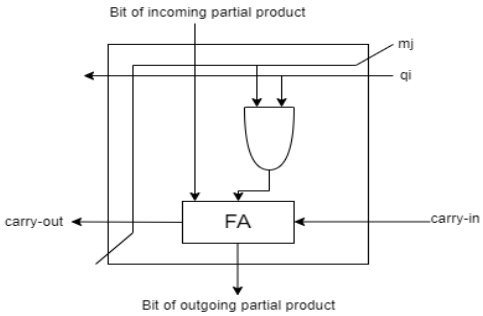

Fig .7 Internal architecture of CSM

The output of the AND gate is given to the reversible full adder which generates the bit of outgoing partial product. The

carry bits from each block's output are transported diagonally downwards to the blocks.

A. CARRY SAVE ADDER

A carry-save adder is a sort of digital adder that can quickly add three or more binary values together. It varies from other digital adders in that it outputs two (or more) values, which can be added together to get the answer to the original summation .

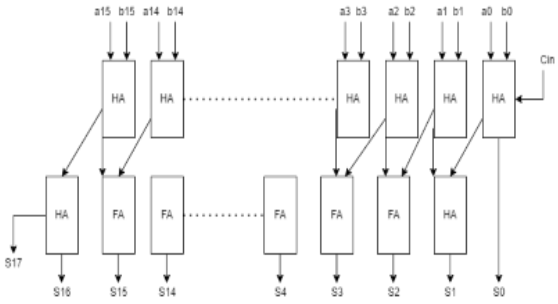

Fig.8 Carry save Adder

Because a binary multiplier includes the addition of more than two binary numbers after multiplication, a carry saving adder is commonly utilized. This method is usually much faster than manually adding those numbers with a huge adder.

VI.REVERSIBLE CONVOLUTION ARRAY ARCHITECTURE

Based on matrix multiplication, this paper proposes a reversible circular convolution.

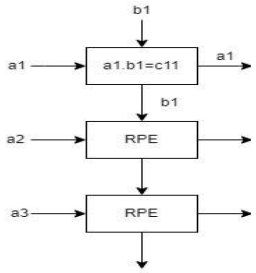

Fig.9 3*1 Reversible Convolution Architecture

As shown in Fig.9, a1, a2, a3 are input response, b1 is an impulse response .Here a1 and b1 gets multiplied and stored in c11, Similarly for next clock cycle, a2 and b1 gets multiplied and stored in c12. The same procedure is repeated for 4*1, 5*1 and 6*1 convolution matrix .

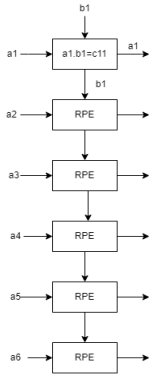

Fig.10 6*1 Reversible Convolution Architecture

Fig.10 shows the convolution matrix for a 6*1 matrix.

VII. RESULTS AND DISCUSSION

Modelsim 5.7g is used to design and simulate the Reversible circular convolution matrix. The performance evaluation of a Full adder, 8bit Multiplier ,Reversible Processing element of a convolution processor has been calculated. The overall architecture's improvement percentage has been calculated.

A.SIMULATION OF CONVOLUTION MATRIX

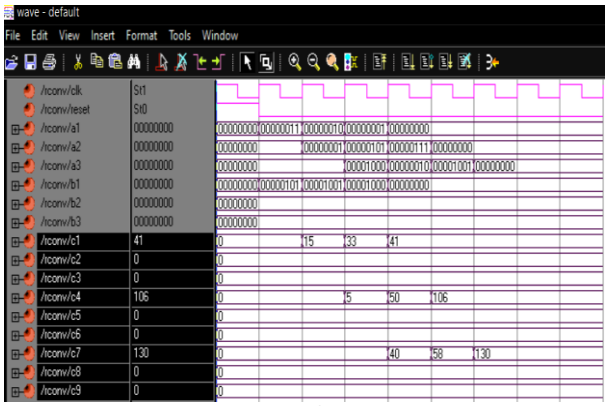

Fig. 11 Simulation result of 3*1 Convolution Matrix

The simulation result of 3*1 convolution matrix shown in Fig 11. depicts how seven clock cycles are required.. The simulation result's test data is presented below.
For the input,
x(n)= {3,1,8}
h(n)={5,9,8}
The output obtained is
y(n) = {41,106,130}

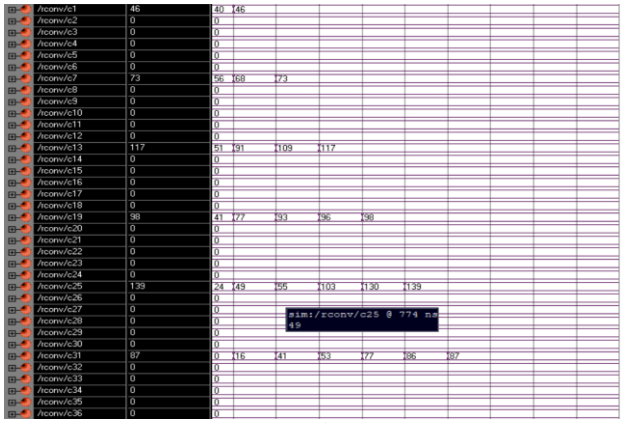

Fig. 12 Simulation result of 6*1 Convolution Matrix

The simulation result of 6*1 convolution matrix shown in Fig 12.. The lag is 13 clock cycles, as shown by the findings. The simulation findings' test results are listed below.

For the input,

x(n)= {2,5,6,4,6,4}

h(n)={4,5,6,8,3,1}

The output obtained is

y(n)= {46,73,117,98,139,87}

B.PERFORMANCE EVALUATION OF FULL ADDER

The results of the fulladder comparison of existing and proposed fulladders are shown in Table 1.

TABLE 1. PE OF FULL ADDER

Methodology	Number of Reversible gates	Quantum Cost	Constant inputs	Garbage outputs
Existing	2	8	1	2
Proposed	2	15	2	4

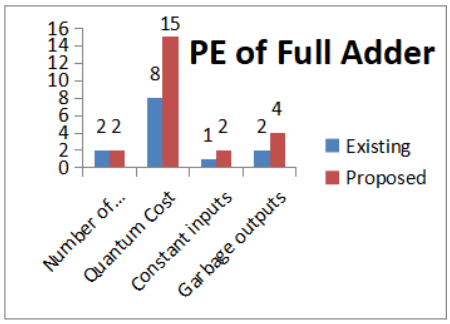

Fig. 13 PE of Full Adder

The graphical representation of PE of Full adder implies that, the number of reversible gates employed in the existing methodology is 2, with a quantum cost of 8, and two garbage outputs. The suggested technique employs two reversible gates with two constant inputs, four garbage outputs, and a quantum cost of fifteen.

CALCULATION

Number of Gates (NOG) = NOG_{P2RG} + $NOG_{FREDKIN}$

= [1(1) +1(1)]

= 2

Garbage output (GO) = GO_{P2RG} + $GO_{FREDKIN}$

= [1(2) +1(2)]

= 4

Quantum Cost (QC) = QC_{P2RG} + $QC_{FREDKIN}$

= [1(10) +1(5)]

= 15

C.PERFORMANCE EVALUATION OF 8bit REVERSIBLE CARRY SAVE MULTIPLIER

Table 2 .compares and contrasts existing and suggested solutions. The Save multiplier is a reversible 8 bit multiplier.

TABLE 2. PE OF 8bit MULTIPLIER

Methodology	Number of Reversible gates	Quantum Cost	Garbage outputs
Existing	513	3333	1026
Proposed	192	1280	256

The graphical representation in Fig.14 depicts the evaluation of 8 bit Multipliers performance in existing and suggested approaches

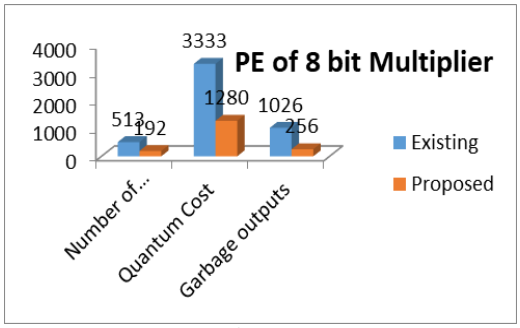

Fig. 14 PE of 8 bit multiplier

The number of reversible gates utilized in the existing methodology is 513, with a quantum cost of 3333, and 1026 garbage outputs. There are 192 reversible gates, 256 trash outputs, and a quantum cost of 1280 in the suggested technique.

CALCULATION

Number of Gates (NOG) = NOG_{FA} + NOG_{AND}

= [64(2) +64(1)]

=192

Garbage output (GO) = GO_{FA} + GO_{AND}

= [64(4) +64(0)]

= 256

Quantum Cost (QC) = QC_{FA} + QC_{AND}

= [64(15) +64(5)]

= 1280

D.PERFORMANCE EVALUATION OF PROCESSING ELEMENT

Table 3 shows the results of the comparison of current and proposed reversible processing elements.

TABLE 3. PE OF REVERSIBLE PROCESSING ELEMENT

Methodology	Number of Reversible gates	Quantum Cost	Garbage outputs
Existing	545	3461	1058
Proposed	224	1312	324

The graphical representation of RPE is shown in Fig.15, which describes the number of reversible gates employed in the existing technique in the RPE module is 545, using 3461 and 1058 as quantum costs 248 reversible gates, 416 trash outputs, and a quantum cost of 1312 are used in the proposed approach.

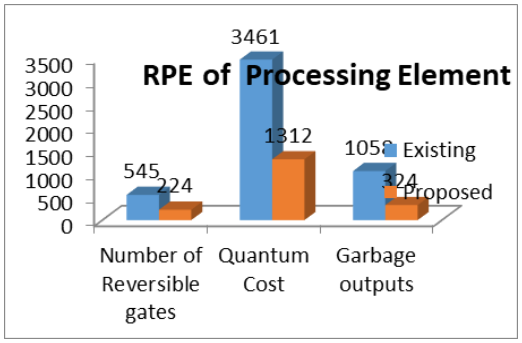

Fig.15 RPE of processing element

E. COMPARISION TABLE

The TABLE 4 shows that , the utilization of number of gates quantum outputs and garbage outputs for 3*1, 4*1, 5*1 and 6*1 Convolution matrices in existing and proposed methodology.

TABLE 4. COMPARISION TABLE

Convolution Range	Existing Methodology			Proposed Methodology		
	Number of Reversible gates	Quantum cost	Garbage outputs	Number of Reversible gates	Quantum cost	Garbage outputs
3x1	1635	10383	3174	672	3936	972
4x1	2180	13844	4232	896	5248	1296
5x1	2725	17305	5290	1120	6560	1620
6x1	3270	20766	6348	1344	7872	1944

The statistics show that the suggested reversible convolution architecture provides improvement in terms of the number of reversible gates, quantum cost, and trash outputs as the architecture grows in size.

F.% OF IMPROVEMENT

Table 5 shows the percentage improvement for each parameter.

TABLE 5. % OF IMPROVEMENT

Parameter	% of Improvement		
	Number of Reversible gates	Quantum cost	Garbage outputs
% of Improvement:	58.89	62.09	69.37

The table 5 infer that, the overall improvement of the proposed convolution architecture with respect to reversible gate, quantum cost, and garbage outputs are 54.49% , 61.83 , 60.68% respectively.

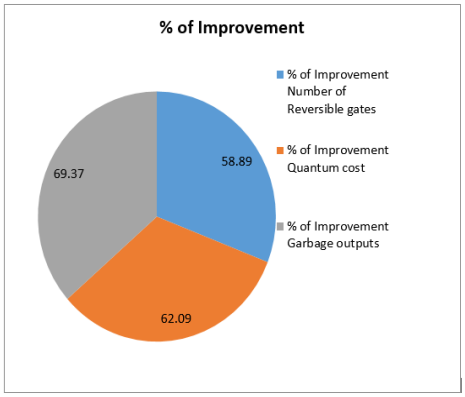

Fig.16 % of improvement

The graphical representation of percent of improvement in Fig.16 displays the overall architecture's percentage of improvement.

G.LOGICAL UTILIZATION

The logic utilization of reversible circular convolution matrix is shown in matrix Table 6.

TABLE 6. LOGIC UTILIZATION

REVERSIBLE CIRCULAR CONVOLUTION ARCHITECTURE	LOGIC UTILIZATION	
	EXISTING	PROPOSED
3*1	2520	1636
4*1	3770	2930
5*1	5360	4600
6*1	7500	6270

The logic utilization has been analyzed and calculated in Quartus 20.2 for 3*1 , 4*1 , 5*1 and 6*1 and the values are found to be 1636, 2930,4600, 6270 respectively.

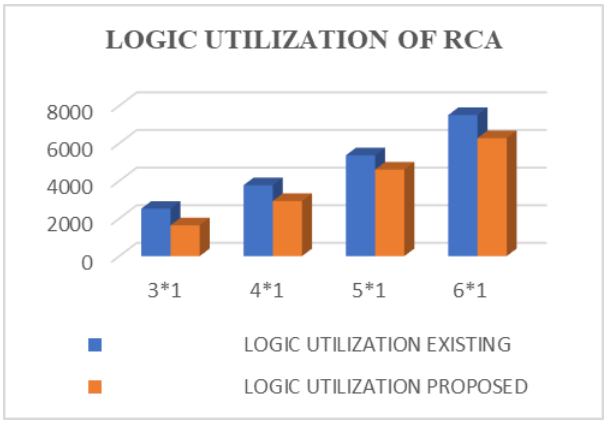

Fig.17 Logic utilization of RCA

The graphical representation in Fig.17,shows the existing and proposed logic utilization of reversible circular convolution architecture.

VIII.CONCLUSION

Speed of Operation and area reduction is perhaps the major concern in most of the DSP applications. This research presents a systolic circular convolution-based approach for matrix multiplication. ModelSim 5.7g was used to build and simulate all systolic architecture modules. Quartus 20.2 synthesis was used to examine parameters logic utilization. It was found that in proposed convolution architecture reversible gate count, quantum cost, and garbage outputs were improved by 58.89% , 62.09%, 69.37% respectively. The projected systolic design will be beneficial to high-speed DSP applications that map high-level computation into hardware structures. Because of its regularity, the systolic system is simple to build and understand. Systolic design can produce cost-effective, high-performance special-purpose computers for a variety of difficulties.

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AUTHORS PROFILE

Mr. Mhaboobkhan.F, currently working as an Assistant professor in P. A. College of Engineering and Technology, Pollachi, Coimbatore. He completed Masters of Engineering in VLSI Design. His research interest are Digital VLSI and Reversible logic. He has published papers in reputed Journals and Conference.

Mrs. Durga devi.M , currently pursuing as an U.G Scholar in P.A College of Engineering and Technology.

Ms. Kaaviyaa.M ,currently pursuing as an U.G Scholar in P.A College of Engineering and Technology.

Ms. Keerthana.G , currently pursuing as an U.G Scholar in P.A College of Engineering and Technology.