International Journal of Advanced Engineering Science and Information Technology (IJAESIT)
ISSN: 2349-3216
Vol.6, No.6, June 2023

A Comprehensive Analysis of Various Multilevel Inverter Topologies: A Critical Assessment

[1]Nithya S
Assistant Professor and EEE
Park College of Engineering and Technology, Coimbatore
Nith48@gmail.com

[2]Padmanabhan B
Associate Professor and EEE
Park College of Engineering and Technology, Coimbatore
Padmanabhan4eee@gmail.com

[3]Vinotha M
Assistant Professor and EEE
Park College of Engineering and Technology, Coimbatore
Vinotha4996@gmail.com

Abstract*— In recent times, multilevel inverters (MLIs) have gained significant prominence as a powerful solution for power conversion in various applications, including flexible AC gearbox systems (FACTS), electric motor drives, renewable energy resources (RERs), and more. These power electronic devices offer various benefits, including decreased switching stress and they are suitable for high voltage and high power applications because they have lower total harmonic distortion (THD) and harmonic interference. As a result, the need for large passive filters is minimized, leading to reduced size and weight. Multilevel inverters are capable of generating nearly sinusoidal output current waveforms, contributing to improved power quality in micro grid systems. The benefits of utilizing multilayer inverters to fewer switches in a circuit, which in turn reduces the need for gate driver circuits, reduces weight, and lowers total harmonic distortion (THD), are covered in detail in this paper. In the study, a five-level inverter is simulated utilizing a variety of pulse width modulation (PWM) methods, and the analysis of their effects on the harmonic spectrum. System modeling is done with MATLAB/SIMULINK. This thesis also includes a comparison of a number of multilevel inverter topologies, including the diode-clamped inverter, the flying capacitor clamped inverter, the cascaded H-bridge inverter, and the asymmetrical MLI.

Keywords—— Multilevel inverter MLI, THD, PWM, CMLI, DMLI, FCMLI.

I. INTRODUCTION

An inverter is an electrical appliance that transforms DC power into AC power at the required output voltage and frequency. In contexts like homes and stores, it is frequently used as a residential emergency backup power source. The need for high power applications has grown in the industrial sector as a result of technological improvements. Multilevel inverters can handle the power demands of such applications, which is where they are useful. Multilevel inverters were first conceptualized in 1975 and Since then, they have received significant interest from the power electronics community. Multilayer inverters have emerged as a crucial component in modern micro grids that incorporate renewable energy sources. In Industrial application, Multilevel Inverter is used in medium and high power application. Multilevel inverters include a number of enticing advantages, such as lower harmonic distortion, more voltage levels, lower harmonic content, and performance flexibility. Lower switching losses, which boost efficiency and cut down on energy waste, better electromagnetic compatibility (EMC),which lessens interference with other systems.

Kouro [2010] reviewed recent developments and commercial uses of multilevel converters (7). A survey of cascade multilevel inverters (10) is provided by Malinowski [2010]. A new multilayer converter topology with fewer power electronic components (4) was put forth by Ebrahimi [2012]. A cascaded multilayer inverter based on a switched capacitor is provided by Jun FengLiu [2014] for use in high frequency AC power distribution systems (5). Using an improved pulse width modulation approach, Prabaharan [2015] investigated a single phase decreased switch count asymmetric multilevel inverter (12). A hybrid PWM technique (13) was used by Prabaharan [2015] to create an asymmetric multilayer inverter arrangement. Using unipolar pulse width modulation techniques, Prabaharan N [2016] compared the performance of symmetric and asymmetric reduced switch multilevel inverter topologies (11). A succinct overview of multilevel inverter topologies (1) is provided by Anjali Krishna [2016]. Krishna Kumar Gupta made a review [2016] insists on a multilayer inverter topology (8) with fewer devices. A redesigned Multilevel Inverter Topology with a Minimal Number of Switches (3) is presented by Addagatla Nagaraju [2017]. A general topology for an asymmetrical multilevel inverter (6) with fewer switches was created by Kamal deep Boora [2017]. Amoul [2017] provides a succinct overview of multilevel (2) inverter topologies. Masoudina [2020] offers a revolutionary cascaded multilevel inverter with electronic components (9) that consume less electricity.

Ⅱ. VARIOUS CLASSIFICATION OF MULTILEVEL INVERTER

Multilevel Inverters can be categorised using different criteria. Some common classifications of multilevel inverters include:

1. Voltage Levels
2. Five-level, seven-level, and higher-level inverters
3. Topology
4. Switching Techniques
5. Application
6. Control Strategies
7.

Multilevel inverters come in a variety of forms, each with a distinct configuration and traits. Multilevel inverter types that are frequently utilized include:

A. *Symmetrical Multilevel Inverter***:** Symmetrical multilevel inverters have many voltage levels. Capable of generating as well as their topology can be used to categories them.
*a)Based on Voltage Levels**:***
i) Two-level Symmetrical Multilevel Inverter**.**
ii) Three-level Symmetrical Multilevel Inverter.
b)Based on Topology:
i) Diode Clamped Multilevel Inverter
ii) Flying Capacitor Multilevel Inverte**r**
iii) Cascading multilevel H-Bridge inverter

B. *Asymmetrical Multilevel Inverter***:** Improved harmonic performance is made possible by this sort of multilevel inverter's utilization of various voltage levels for the Output waveform's positive and negative half-cycles. Applications requiring a high-quality output waveform and little harmonic distortion are appropriate for it.

C. *Hybrid Multilevel Inverter:* This type of multilevel inverter combines two or more types of multilevel inverters to leverage their advantages and overcome their limitations. It can provide improved performance in terms of output waveform quality, efficiency, and harmonic performance. These are a few of the most typical varieties of multilevel inverters, each with unique benefits and drawbacks. Depending on the particular needs of the application, such as the desired output waveform quality, voltage level, and harmonic performance, the right type of multilevel inverter must be chosen.

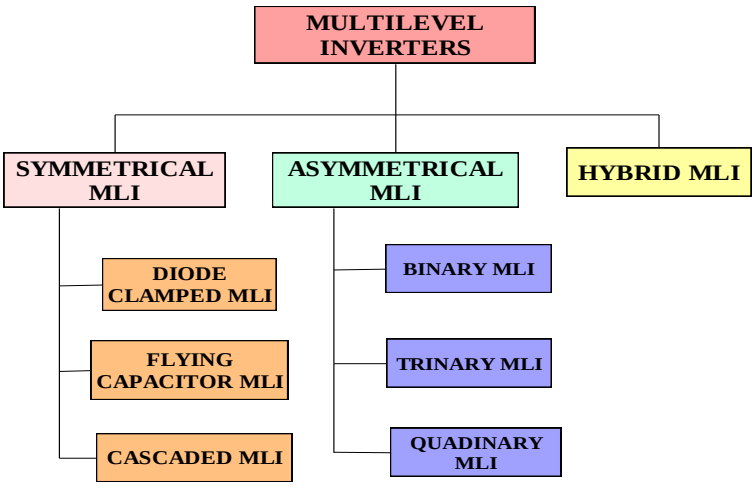

Figure 1 Multilevel Inverters type

Ⅲ. TOPOLOGIES OF MULTILEVEL INVERTER

The characteristics of the source voltages used determine the multilayer inverter topologies can be roughly divided into hybrid inverters, asymmetrical inverters (with unequal source voltages), and multilevel multisymmetric inverters.

A.MULTILEVEL MULTISYMMETRIC INVERTER:

A multilevel multisymmetric inverter is characterized by having voltage sources with equal amplitudes. For instance, if a DC source of 100V is used for one level, then all the other inverter levels will also have sources with 100V amplitude.

i. Diode-Clamped Multilevel Inverter

The symmetrical multilevel inverter's fundamental principle in order to reduce the voltage stress on power components, diodes should be used. The inverter's switches and capacitors each have a voltage of Vdc. Two (m-1) Changing gadgets, (m-1) capacitors, (m-1)(m-2) diodes, and (m-1)(m-1) voltage generators are needed for each leg of an m-level inverter.

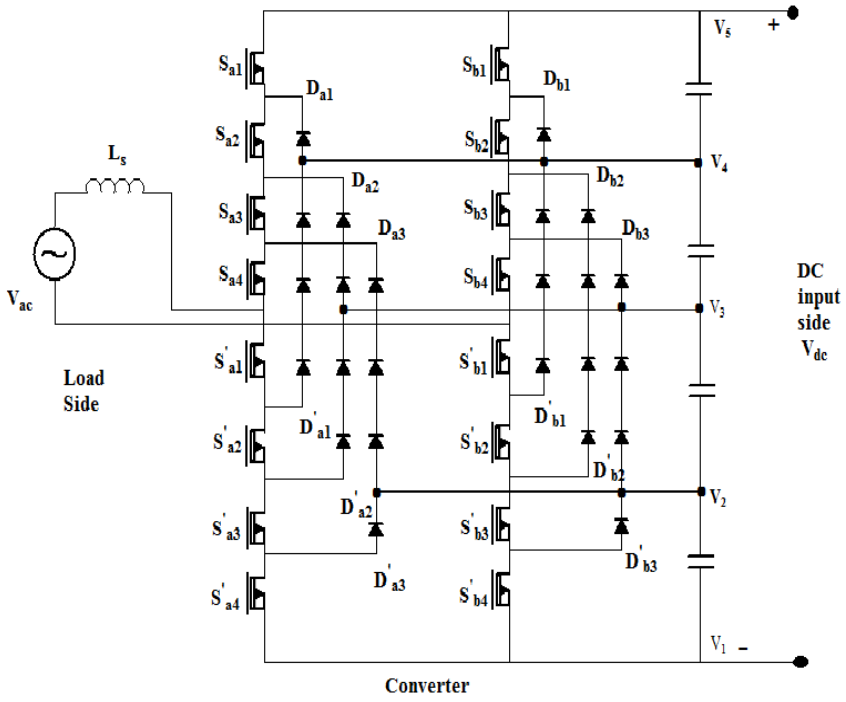

Figure 2 Five level Diode Clamped Multilevel Inverters

a) Principle of operation:

To generate a voltage stair-step in a five-level inverter, let's only one inverter leg should be thought of an example, as depicted in Figure 2. Figure 3 shows a single-phase bridge with two legs. The reference point for the output phase potential is the dc rail 0.

The five-level voltages are created using the following steps:

1. To achieve an output voltage level of va0 = Vdc, turn on all upper-half switches Sa1 through Sa4.
2. To obtain an output voltage level of va0 = Vdc/2, turn on two upper switches Sa3 through Sa4 and two lower switches S'a1 and S'a2.
3. Switch on each bottom half switch individually, S'a1 through S'a4, to provide output voltage va0 = 0.

Each switch has two states in the multilayer State 1 of the inverter denotes that the switch is turned on, while State 0 denotes the toggle is closed.. It is significant to note that there are four complimentary switch pairs in each phase and that each switch is only activated once every cycle. These pairs are Sa1, Sa1, Sa2, Sa2, Sa3, Sa3, and Sa4 all refer to the same thing for one leg of the inverter. The voltages at terminals a and b's positive and negative phase legs, respectively combine to form the inverter's line voltage. It is the line voltage represented by a five-story stairwell wave because each phase-leg voltage follows one-half of the sinusoidal waveform. According to this, an (2m-1) level output

line voltage of an m-level inverter as well as a m level output phase-leg voltage.

The calculation of the switching angles should be done in a way that minimizes the appearance of lower dominant harmonics in order to produce minimal total harmonic distorting the output voltage (THD). The switching angles in multilayer inverters are frequently calculated using the harmonic elimination approach. By selecting the proper switching angles when the inverter is operating, this technique enables the elimination of particular harmonics.

(b) Features of Diode Clamped Multilevel Inverter:

1. High-voltage rating required for blocking diodes:
2. Unequal device rating
3. Capacitor voltage unbalance

(c) Advantages:

1. High efficiency**:**
2. Filters are not required to minimise harmonics

(d) Disadvantages:

1. More diodes are need for high levels

ii. Flying Capacitors Multilevel Inverter:

Similar flying capacitor multilayer inverter divides the input DC voltage among capacitors is used to regulate the voltage applied across power devices. The topology's switches and capacitors all operate at Vdc voltage. The flying capacitor-based multilevel inverter's structure is seen in Figure 3.where each to a multilayer inverter with diode clamping, the level converter's DC bus must include (m-1) capacitors

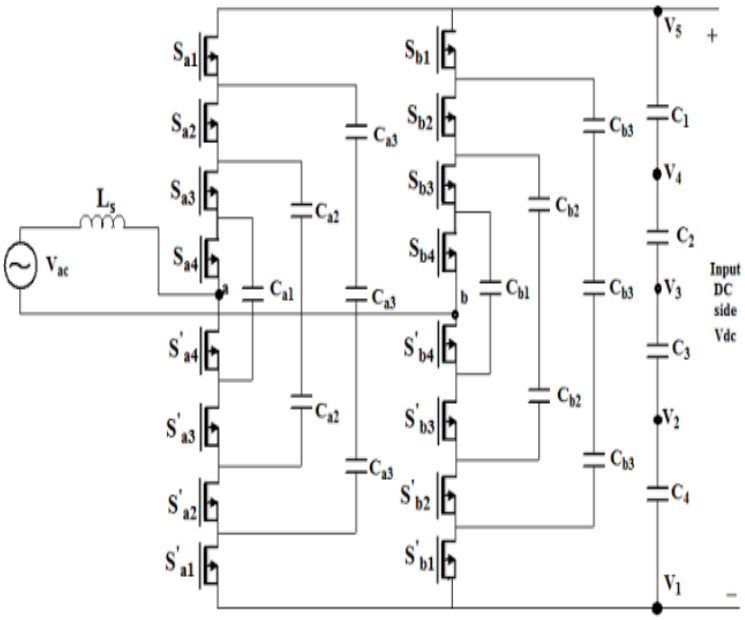

Figure 3 Flying multilayer inverter using capacitors with five levels.

(a) Features of Flying Capacitor Multilevel Inverter:

1. Uses a lot of capacitors
2. Requires balancing of capacitor voltages

(b) Advantages

1. An additional ride-through option for power outages
2. Harmonics reduction with no filters applied.

(c) Disadvantages:

1. High levels demand big numbers of capacitors

2. High switching frequency and transmission losses for actual power

iii. Cascade Multilevel Inverter With Separate DC Sources

The idea behind the flying capacitor multilayer inverter is to create a sinusoidal voltage output by series-connecting H-bridge inverters. The inverter's output voltage is the sum of the voltages produced by each of its n cells, and there are 2n+1 levels of output voltage in total. Improved power quality can be achieved by selecting the switching angles a technique that lessens the output waveform's complexity of the cells overall harmonic distortion. Flying capacitor multilevel inverters have the advantage of requiring fewer components than multilayer inverters with diode-clamped or flying capacitors, which are less expensive and lightens the inverter's weight. This can be beneficial in terms of system affordability, ease of installation, and transportation.

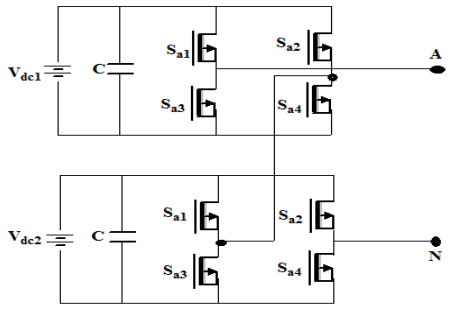

Figure 4 Inverter with five levels of cascading levels

Fig. 4 shows a five-level cascaded H-bridge multilevel inverter. This inverter's approach for calculating switching angles is similar to that of earlier multilayer inverters. Two (m-1) switching devices are needed for an, where m is the number of output voltage levels. This inverter Multilevel H-bridge inverter with m levels in cascade has the benefit of not requiring additional voltage balancing capacitors or clamping diodes, which simplifies the overall design and lowers the component count.

The cascaded H-bridge multilevel inverter is a typical structure for reaching high voltage levels with fewer harmonics in the output waveform. By modifying the switching angles of the individual H-bridge cells, the output voltage may be synthesised to create a multi-level waveform, which enhances power quality and reduces harmonic distortion. The multilevel cascaded H-bridge inverter system's best performance depends on careful switching angle selection, component sizing, and control technique.

(a). Features of Cascaded Multilevel Inverter:

1. The multilayer inverter can be powered by a variety of DC sources, including biomass, PV, and fuel cells.
2. Due to limitations or design restrictions, it is not possible to connect the two converters back-to-back, which entails connecting the output of one converter to the input of another.

(b). Advantages:

1. Compared to other types of inverters, fewer the same number of voltage levels can be achieved with the same number of components. No additional diodes or capacitors are required simplifying the circuitry and reducing component count.
2. The consistent structure of the multilevel inverter allows for a scalable and modularized circuit layout and packaging, facilitating ease of implementation and customization.

(c). Disadvantages:

1. The multilayer inverter requires dedicated and distinct DC sources for actual power conversion, as each level of the inverter requires its own supply of DC voltage.

B. ASYMMETRICAL MULTILEVEL INVERTER:

*i. Binary Multilevel Inverter**:***

The cascaded H-bridge multilevel inverter you described in Fig. 1 uses binary DC input sources to synthesise various voltage at output levels. The circuit uses two sets of H-bridge inverters to produce stepped waves. The higher inverter adds or subtracts one level from the lower inverter to create a fundamental output voltage with two levels. According to Equation (1). The terminal voltages of the H-bridge modules are added to produce the final output voltage.Equation (2) states what the anticipated output voltage level "Vn" will be in this circuit architecture if there are

A series of powers of 2 for "n" number of H-bridge modules with separate DC sources:

$$Vout = VHB1 + VHB2\ldots \quad (1)$$

$$Vn = 2^n, \text{ where } n = 1, 2, 3... \quad (2)$$

This indicates that the multilevel inverter's output potential levels will be multiples of 2 raised to the power of "n," where "n" denotes how many cascaded H-bridges there are modules that are being employed.

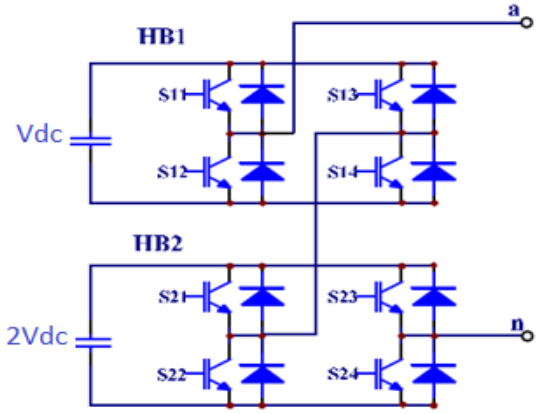

Figure 5 Binary DC source MLI

ii. Trinary Multilevel Inverter:

The cascaded H-bridge multilevel inverter you described in Fig. 6 uses trinary DC input sources to synthesise different output voltage levels. The circuit employs two sets of H-bridge inverters, with the bottom inverter producing a basic the top inverter synthesises stepped waves by adding or subtracting one level from the fundamental wave, and the output voltage has three levels. The final output voltage, according to equation (3), is the sum of the terminal voltages of the H-bridge modules.

$$Vout = VHB1 + VHB2\ldots \quad (3)$$

Equation (4), for this circuit design, predicts if there are "n" H-bridge modules with separate DC sources, the anticipated output voltage level "Vn" will be in a series of powers of 3.

$$Vn = 3^n, \text{ where } n = 1, 2, 3... \quad (4)$$

This indicates that the multilevel inverter's output potential levels will be multiples of 3 raised to the power of "n," where "n"denotes how many cascaded H-bridges modules employed.

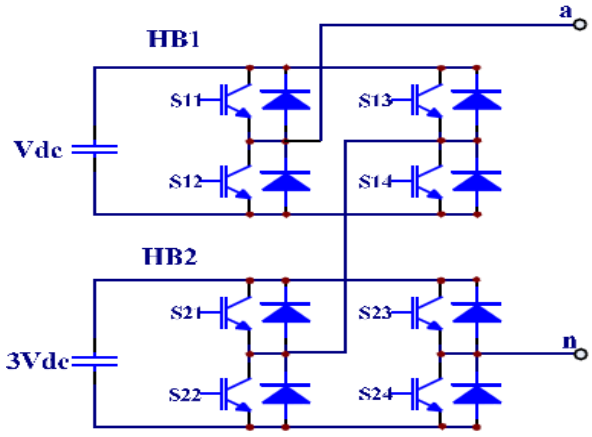

Figure 6 Trinary DC source MLI

In Fig. 7, it appears that the Fast Fourier Transform (FFT) window in MATLAB/Simulink is being used to examine the harmonic spectra of a trinary DC source multilevel inverter (MLI). A popular signal processing method for examining a signal's frequency components is the FFT. The harmonic spectrum can be produced by applying the Window FFT in to the output waveform of the MATLAB/Simulinktrinary DC source MLI.

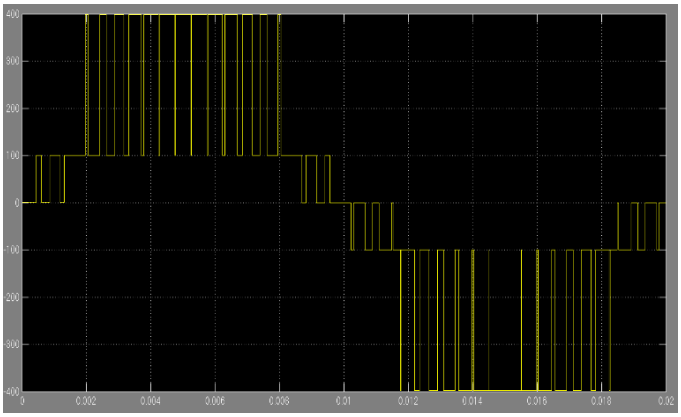

Figure 7 Simulation of five level trinary multilevel Inverter

iii. *Quadinary Multilevel Inverter*

The schematic diagram for a cascaded H-bridge multilevel inverter with a quadratic DC input source can be seen in Fig.8. With different input DC sources, this configuration is comparable to a conventional multilayer H-bridge inverter with cascading. By using Vdc and 4Vdc as input voltages, this multilevel inverter can generate five different output voltage levels: -4Vdc, -Vdc, 0, VdcandVdc.

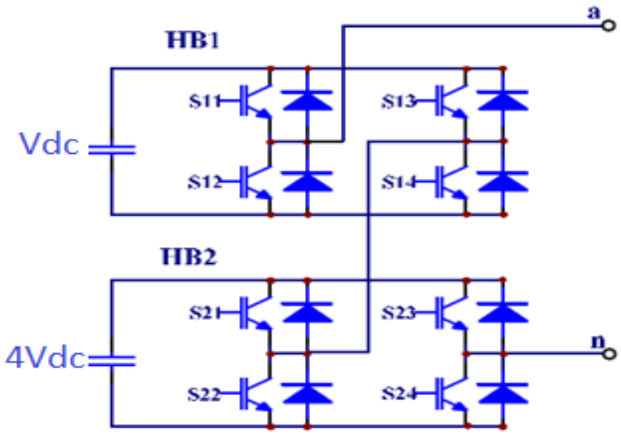

Figure 8 Quadinary DC source MLI

In the suggested circuit topology with quadrilateral DC input sources, the lower inverter generates a fundamental output voltage with four levels, and the higher inverter adds or subtracts one level from the fundamental wave to synthesise the stepped waves. According to equation (5), the ultimate output voltage equals the sum of the terminal voltages of the H-bridge modules

Vout = VHB1 plus VHB2…(5)

where the voltages at the lower and higher H-bridge terminals modules, respectively, are VHB1 and VHB2, respectively. If there are n H-bridge modules with independent DC sources and the DC sources have a series of powers of 4, then the expected output voltage level is provided by equation (6) based on this circuit topology:

For n = 1, 2, 3, Vn = 4n...(6)

IV.SIMULATION RESULTS

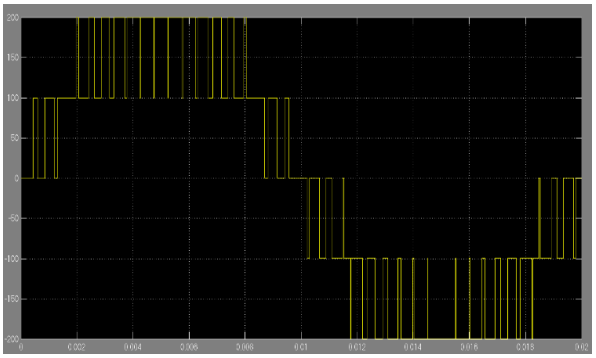

Figure 9 Simulation of Inverter with five levels of cascading levels

Eight ideal switches are used in the simulated model shown in the figure below. For proper control in real-world scenarios, each of these switches would need its own gate driver circuit. A 10 ohm load is utilised in conjunction with a 100 volt DC power source. Prior to using by comparing a triangle waveform with a fixed value at predefined time intervals during simulations using multicarrier PWM techniques, a separate multistep output waveform was produced. The harmonic spectrum was further analysed using MATLAB / Simulink's FFT Window based on the selected PWM techniques.

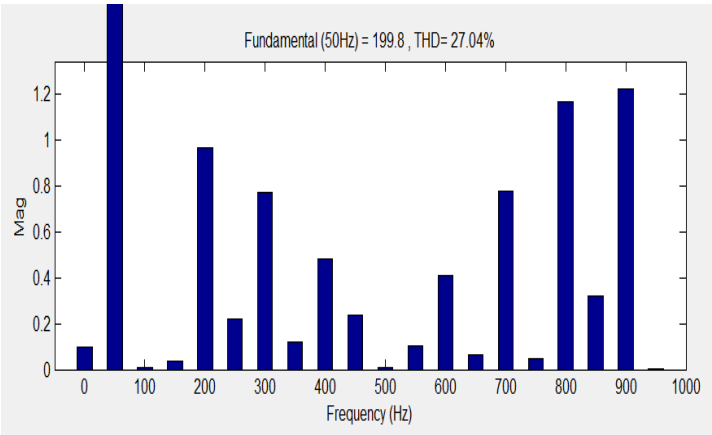

Figure 10 THD for Inverter with five levels of cascading levels

Phase a	**S_a**	**S_1**	**S_2**	**S_3**	**S_4**
$2V_{dc}$	Off	On	On	Off	Off
V_{dc}	On	Off	Off	Off	Off
0	Off	Off	Off	Off	On
$-V_{dc}$	On	Off	On	Off	Off
$-2V_{dc}$	Off	Off	Off	On	On

Table 1 Switching State

V. COMPARISON BETWEEN VARIOUS TYPES OF MULTILEVEL INVERTER

Comparison of several multilevel inverter types, including binary multilevel inverters, quandary multilevel inverters, flying capacitor multilevel inverters, and diode clamped multilevel inverters. In terms of the quantity of switching components like main Diodes, balancing capacitors, Dc bus capacitors, and clamping diodes.DCMLI and FCML have Thirty two main switching device and others have sixteen main switching devices. Diode Clamped Multilevel Inverter has fifty six clamping diodes while other devices have none. While other multilevel inverters have zero balancing capacitors, the Flying capacitor Multilevel Inverter has fifty six. Others have four, whereas DCMLI and FCMLI have eight DC bus capacitors. Every type of MLI has thirty two primary Diodes.

Components	DC MLI	FC MLI	CMLI	Binary MLI	Trinary MLI	Quadinary MLI
Main switching devices	32	32	16	16	16	16
Clamping diodes	56	0	0	0	0	0
Balancing capacitors	0	56	0	0	0	0
DC bus capacitors	8	8	4	4	4	4
Main diodes	32	32	32	32	32	32

Table 2 Comparison Of Component Requirement For Nine Level MLI

VI. CONCLUSIONS

Cascaded multilevel inverters are well known for their benefits in terms of lower component count, easier control, smaller size and installation area, and scalability to meet rising demand in the recommended circuit layout. With fewer semiconductor switches, cascaded multilevel inverters can achieve higher stepped output voltage levels. They are more versatile than other types of multilevel inverters, making them suitable for a range of applications. Additionally, numerous cutting-edge topologies. Cascaded multilayer inverters are an effort to further reduce the number of switching components while maintaining the required output voltage levels. According to simulation results discussed in the paper, multicarrier methods that use pulse width modulation (PWM) can reduce total harmonic distortion (THD) than PWM techniques using triangular or constant values. The occurrence of lower order harmonics may increase with an amplitude modulation index less than unity, rendering it inappropriate for filter construction. Therefore, for achieving a desired output waveform quality with low THD, it would be ideal to have an amplitude modulation index of one or less. In conclusion, cascaded multilevel inverters can increase performance regarding the output waveform's qualityand THD due to their advantages in terms of reduced component count, easier control, and scalability, as well as the use of appropriate PWM techniques and amplitude modulation index

REFERENCES

1. *Anjali Krishna R. and Dr L Padma suresh "A brief review on multilevel inverter topologies" Conference on Circuit, Power and Computing Technologies [ICCPCT] 2016.*
2. *Amoul K. Koshti and M.N. Rao, "A Brief Review of Multilevel Inverter Topologies," 2017 International Conference on Data Management, Analytics and Innovation (ICDMAI) Date of Conference: 24-26 February 2017Date Added to IEEE Xplore: 19 October 2017, ISBN Information: INSPEC Accession Number: 17279666, DOI: 10.1109/ICDMAI.2017.8073508,2017.*

3. *Addagatla Nagaraju and Akkela Krishnaveni "Modified Multilevel Inverter Topology with Minimum Number of Switches" IJSTE International Journal of Science Technology & Engineering volume 3 issue 09 March 2017.*
4. *Ebrahimi J, Babaei E, Goverg Gharehpetian B. A New MultilevelConverter Topology with Reduced number of Power Electronic Components. IEEE Trans. on Ind. Elec., 2012; 59(2):655-667.*
5. *Jun Feng Liu, K.W.E Cheng, A cascaded multilevel inverterbased on switched capacitor for High frequency AC Power Distribution system IEEE Trans. on Power Electron., vol. 29, no.8. , Aug. 2014.*
6. *Kamaldeep Boora and Jagdish Kumar "General topology for asymmetrical multilevel inverter with reduced number of switches" IET Power Electronics 2017.*
7. *Kouro S, Malinowski M, Gopak Umar K,. Pou J, Franquelo L G, W. Bin, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," IEEE Trans. Industrial Electronics, vol. 57, no, 8, pp. 2553-2580, 2010.*
8. *Krishna Kumar Gupta, AlekhRanjan, PallaveeBhatnagar, Lalit Kumar Sahu and Shailendra Jain: Multilevel Inverter topologies with reduced device count: A Review. IEEE Transactions on Power Electronics (Volume: 31, Issue: 1, Jan. 2016)*
9. *Masoudina, F.; Babaei, E.; Sabahi, M.; Alipour, H, "New Cascaded Multilevel InverterWith Reduced Power Electronic Components"Iran. J. Electr. Electron. Eng. 2020, 16, 107.*
10. *Malinowski M, Gopakumar K, Rodriguez J and Peres M A, A survey on cascade multilevel inverters, IEEE Trans. Ind. Electron, vol. 57, n. 7, July 2010, pp.2197-2206.*
11. *Prabaharan N., and Palanisamy K.: Comparative Analysis of Symmetric and Asymmetric Reduced Switch Multilevel Inverter Topology UsingUnipolar Pulse Width Modulation Strategies. IET Power Electronics, DOI: 10.1049/iet-pel.2016.0283.*
12. *Prabaharan N., and Palanisamy K.: Investigation of single phase reduced switch count asymmetric multilevel inverter using advanced pulsewidth modulation Technique. International Journal of Renewable Energy Research, vol. 5, no.3, pp. 879–890, (2015).*
13. *Prabaharan N., Palanisamy K., and Rini Ann Jerin A.: Asymmetric Multilevel Inverter Structure with Hybrid PWM Strategy. InternationalJournal of Applied Engineering Research, vol. 10, no. 55, pp. 2672- 2676, (2015).*

Authors Profile

S.Nithya, Assistant Professor, Department of Electrical and Electronics Engineering, Park College of Engineering and Technology, Coimbatore, India. She completed her Master of Engineering in Power Electronics and Drives from Arunai Engineering College, Thiruvannamalai in 2014 and Bachelor of Engineering in Electrical and Electronics Engineering from Arunai Engineering College, Thiruvannamalai in 2011. She has 6 year experiences in this field and attended many International and National Conference, Workshops and published peer journal. Her current areas of research are Power Electronics, Renewable Energy, Power System, etc.

Dr. B.Padmanabhan received his Ph.D. degree in Faculty of Electrical Engineering from Sathyabama Institute of Science and Technology, Chennai and also he is presently working as Associate Professor in the Department of Electrical & Electronics Engineering, Park College of Engineering and Technology, Coimbatore, India. He has contributed more than 10 peer reviewed journal and International Conference publication. His current research interest includes Power System Optimization, Distributed Generation, Renewable Energy, Smart Grid, etc.

Vinotha M is currently working in Park Engineering of College and Technology as Assistant Professor in the department of Electrical and Electronics Engineering. She has published a paper in the journal. Her area of interest includes generation, transmission and distribution in power system.